Memory cells

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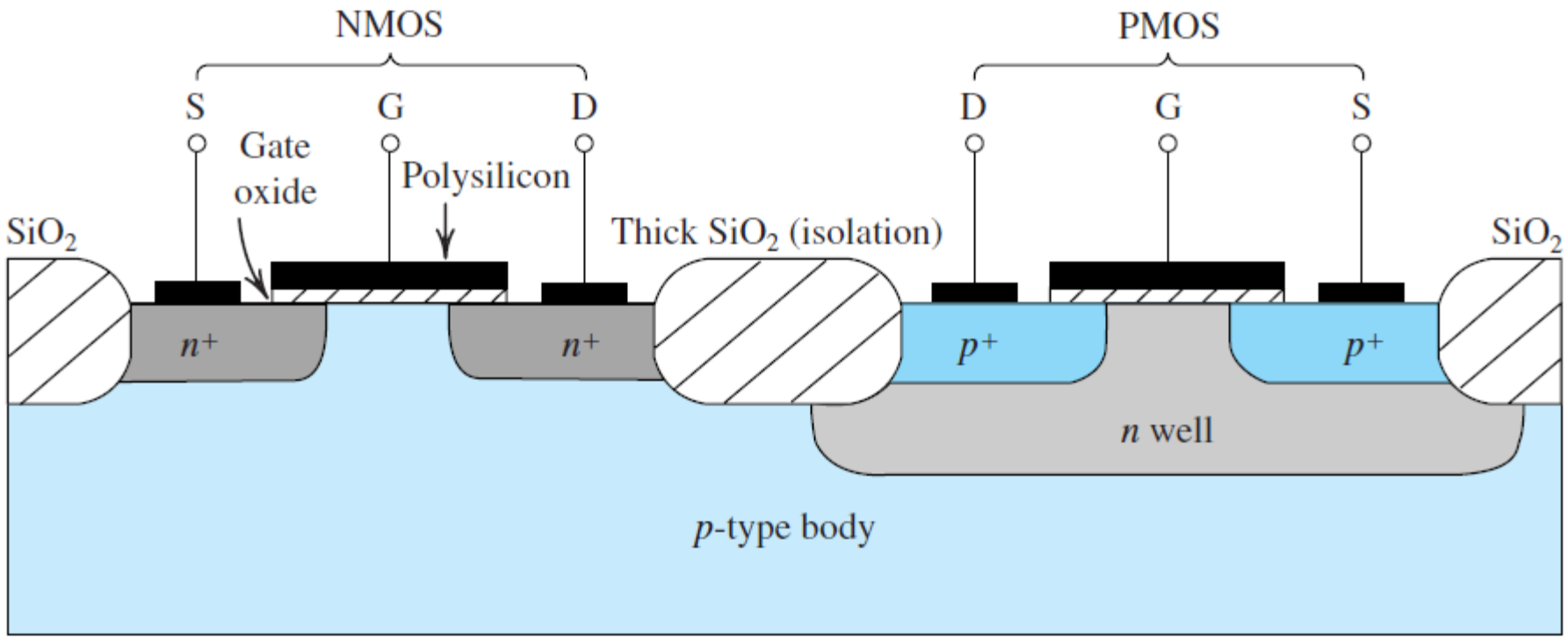
06/25/2021

Transistors



CMOS

logic inverters $Y = \overline{X}$

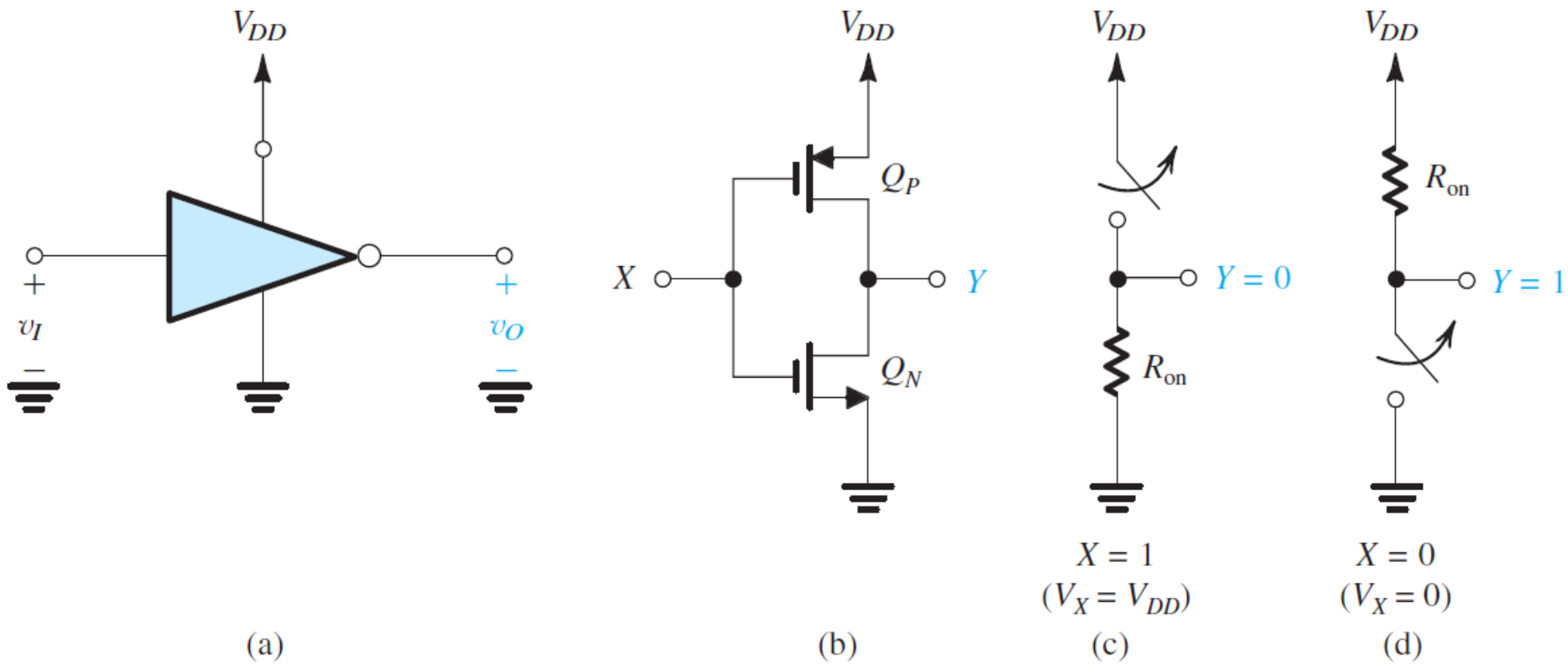


Figure 14.2 (**a**) Block representation of the logic inverter; (**b**) its CMOS realization; (**c**) operation when the input is a logic 1; (**d**) operation when the input is a logic 0.

The Latch

basic memory element

logic inverters

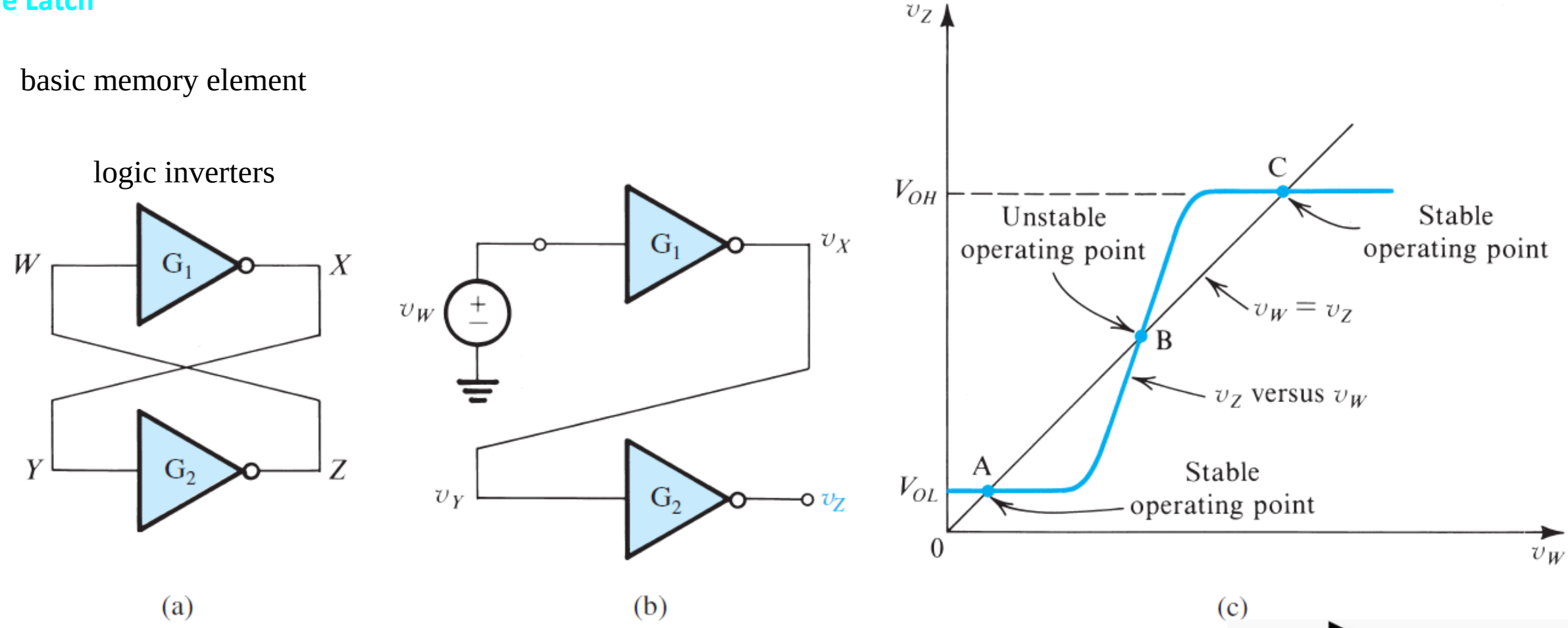
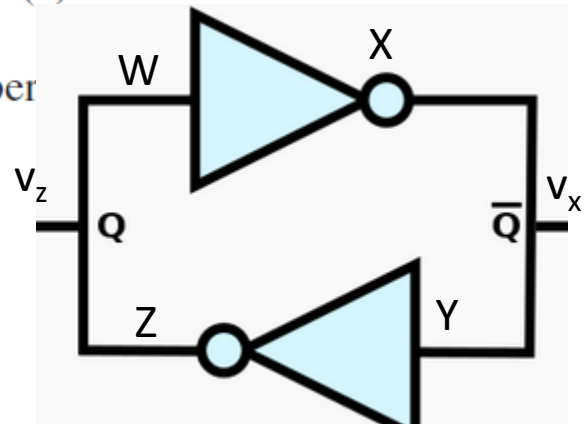


Figure 16.1 (**a**) Basic latch. (**b**) The latch with the feedback loop opened. (**c**) Determining the oper point(s) of the latch.



B + a positive increment → C

a **bistable** circuit: v_w low, v_x high, v_z low, for a stored logic 1

The set/reset (SR) Flip-Flop

The Two-Input NOR Gate

$$Y = \overline{A + B} = \overline{A}\,\overline{B}$$

Input		Output
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

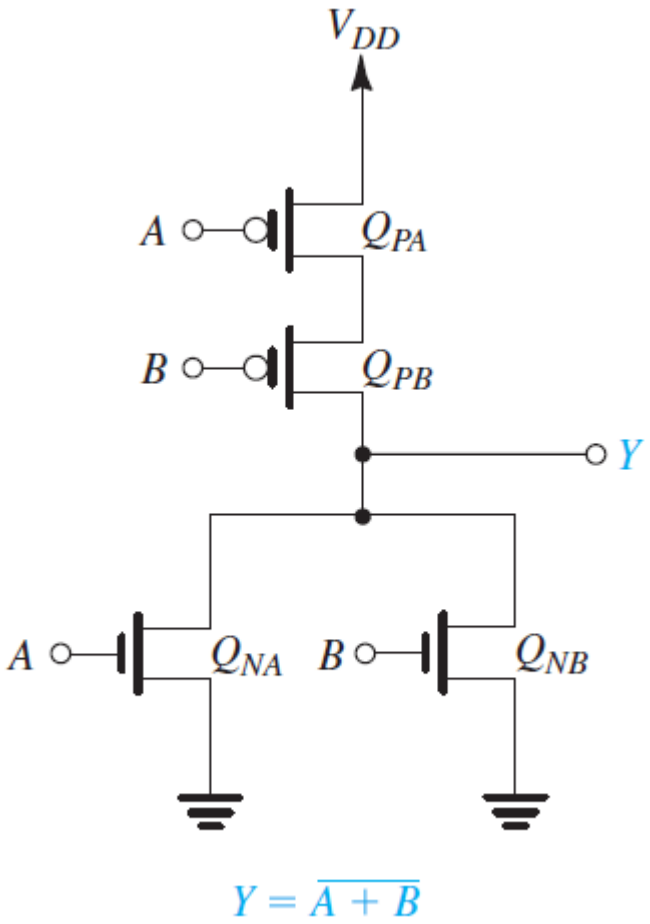
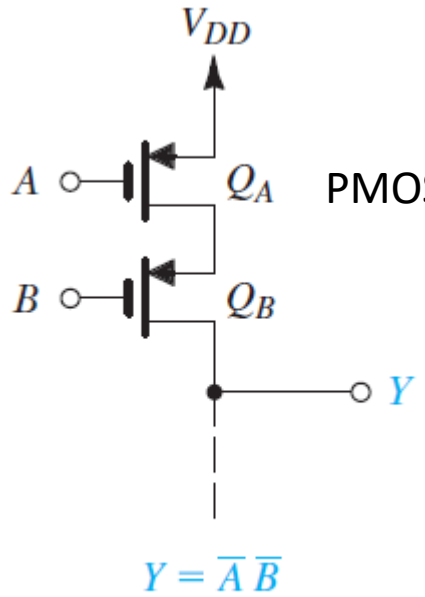


Figure 14.7 A two-input CMOS NOR gate.

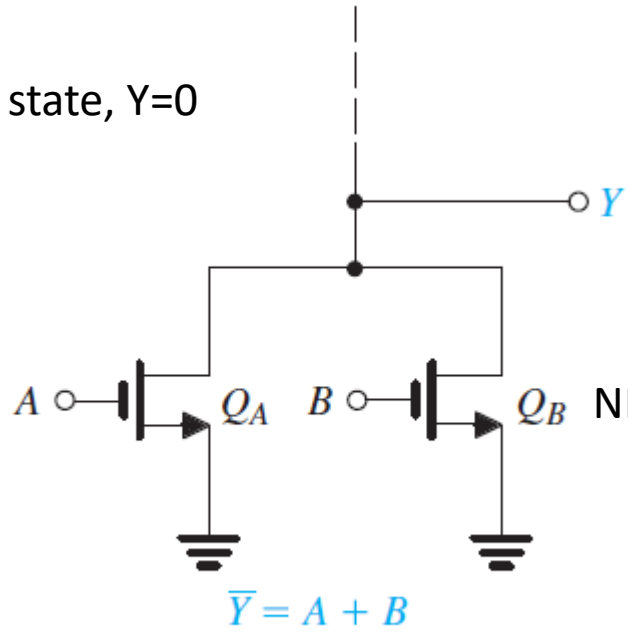
A=1, B=1, Q_{PA} *and* Q_{PB} is OFF state, Q_{NA} *and* Q_{NB} is ON state, Y=0
A=0, B=0, Q_{PA} *and* Q_{PB} is ON state, Q_{NA} *and* Q_{NB} is OFF state, Y=1



PMOS: "high" gate, OFF state

(b)

A=1, B=1, OFF state, Y=0



NMOS

(a)

A=1, B=1, ON state, Y=0

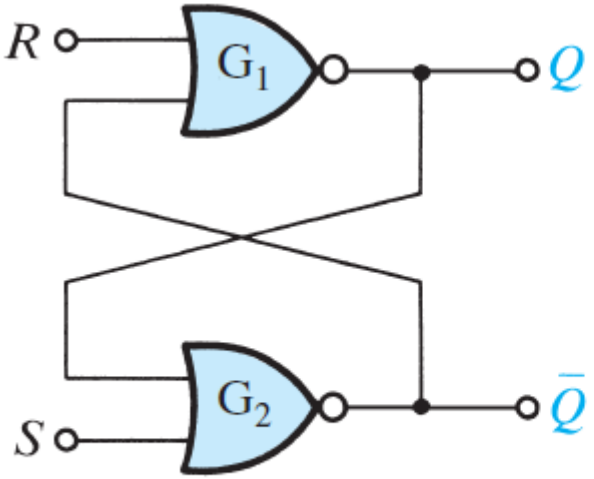
The set/reset (SR) Flip-Flop

The Two-Input NOR Gate

$$Y = \overline{A + B} = \overline{A}\,\overline{B}$$

Input		Output
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

flip-flop: cross-coupling two NOR gates



(a)

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	Not used

(b)

G_1 and G_2 are trigger inputs of the flip-flop.

logic 1: Q is high and $\bar{Q}$ is low

For example, when the flip-flop is storing a logic 0,
$Q = 0, \bar{Q} = 1$
We want to set the flip-flop as a logic 1,
Raise S=1, leave R=0,
It forces $\bar{Q} = 0$, then $Q = 1$

R	S	Q	$\bar{Q}$	
0	0	0	1	*memory state*
0	0	1	0	*memory state*
1	0	0	1	logic 0
0	1	1	0	logic 1
1	1	0	0	

Memory-Chip Organization

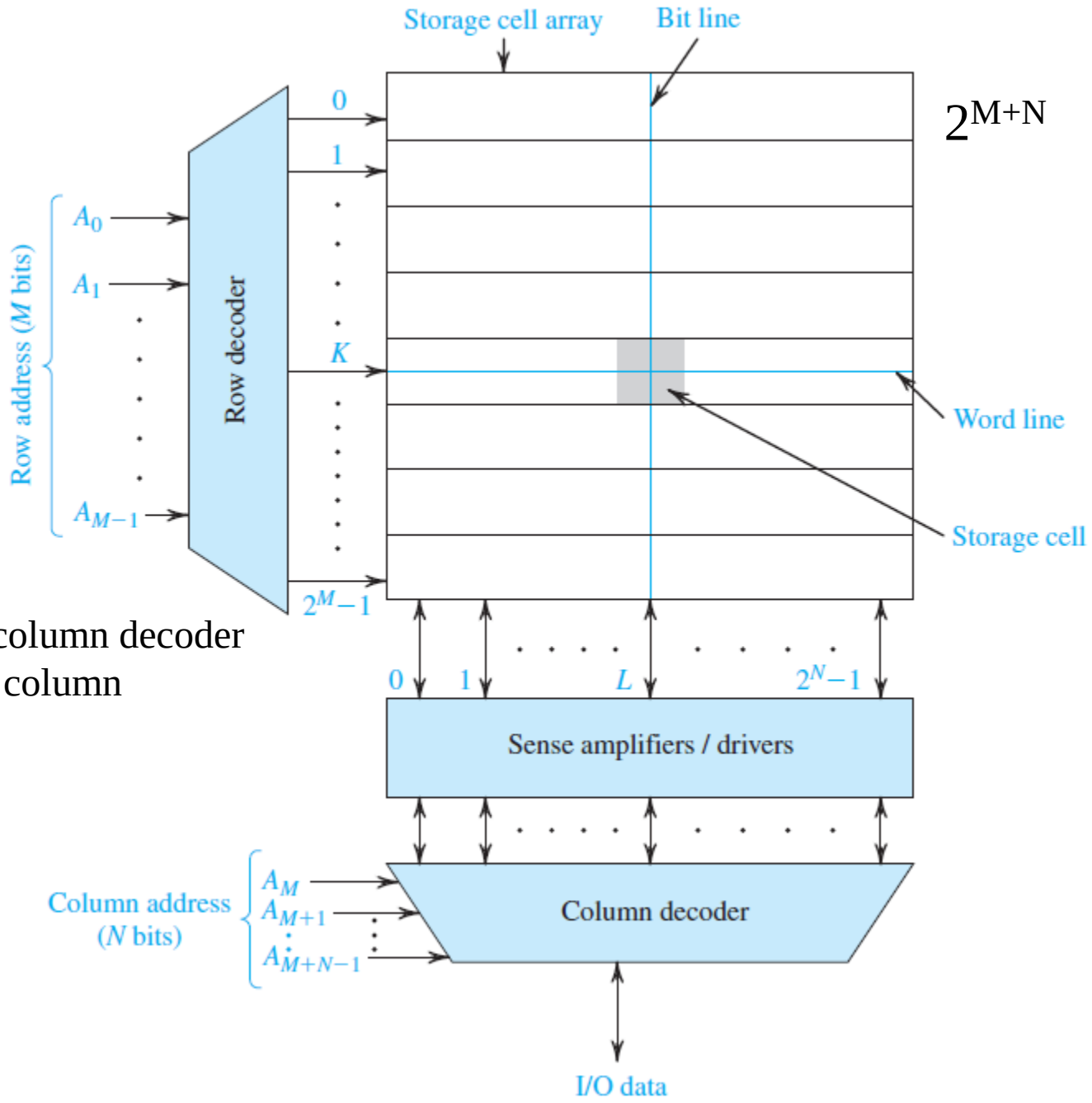
The bits on a memory chip are addressable individua

A 64-Mbit chip needs a 26-bit address (2^{26} = 67,108,864 = 64M).

One bit is stored in one memory cell

A read operation:
Activate *K*th word line,
All cells in row *K* will provide contents to the bit lines,
The small readout signal is amplified and delivered to column decoder
The column decoder selects the signal of the particular column

A **write operation:**
similar



Random-Access Memory (RAM) Cells

two types of MOS RAM:
Static RAMs utilize static latches as the storage cells.
Dynamic RAMs store the binary data on capacitors.

static RAMs can hold their stored data indefinitely, provided the power supply remains on;
dynamic RAMs require ***periodic refreshing*** to regenerate the data stored on capacitors

Both static and dynamic RAMs are *volatile;* they require the continuous power supply.

Static Memory (SRAM) Cell

a flip-flop

6T cell

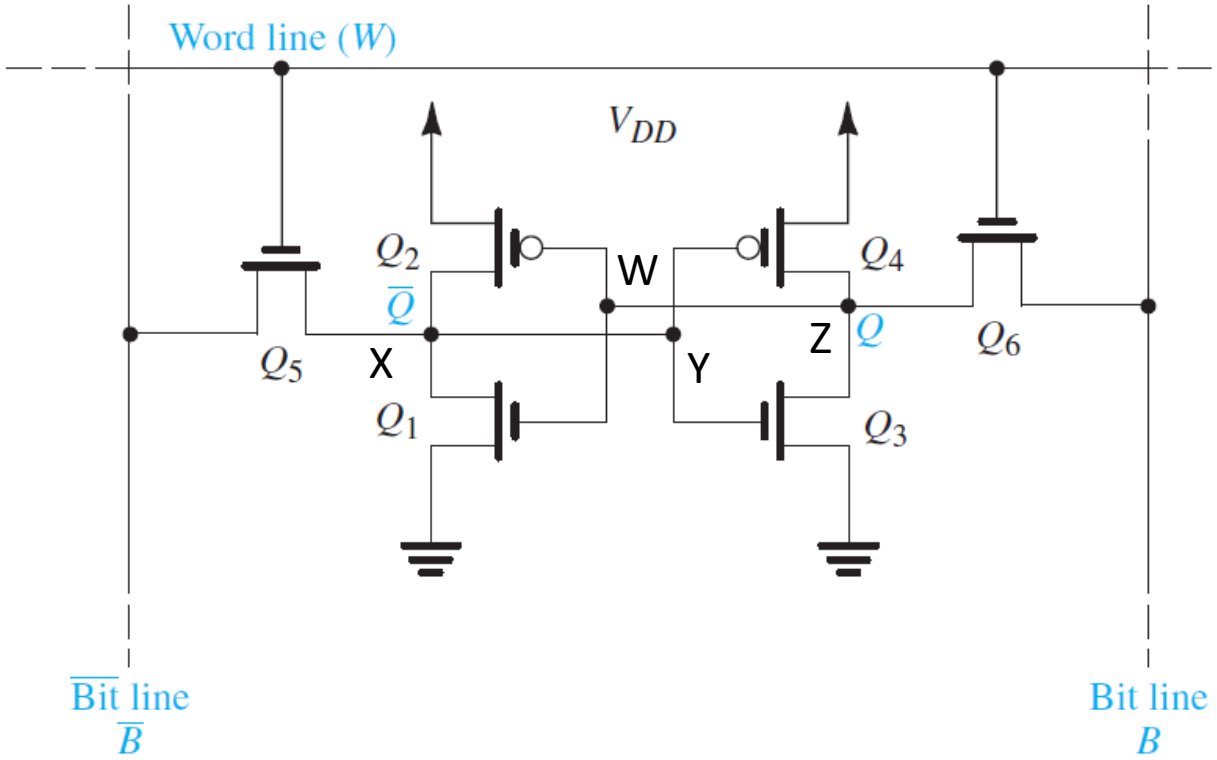
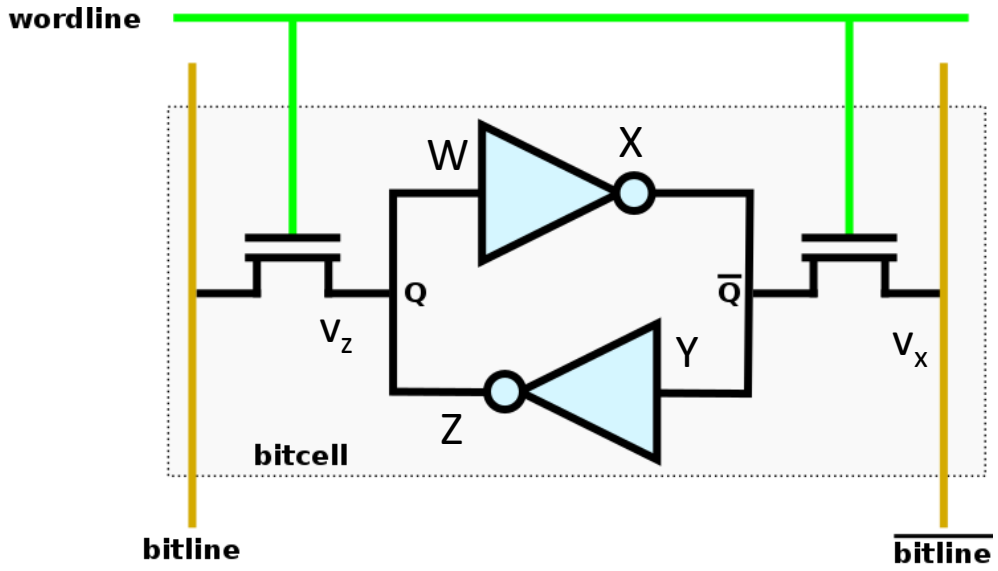


Figure 16.12 A CMOS SRAM memory cell.



The access transistors, Q_5 & Q_6, are turned on when the word line is selected

Static Memory (SRAM) Cell

a flip-flop

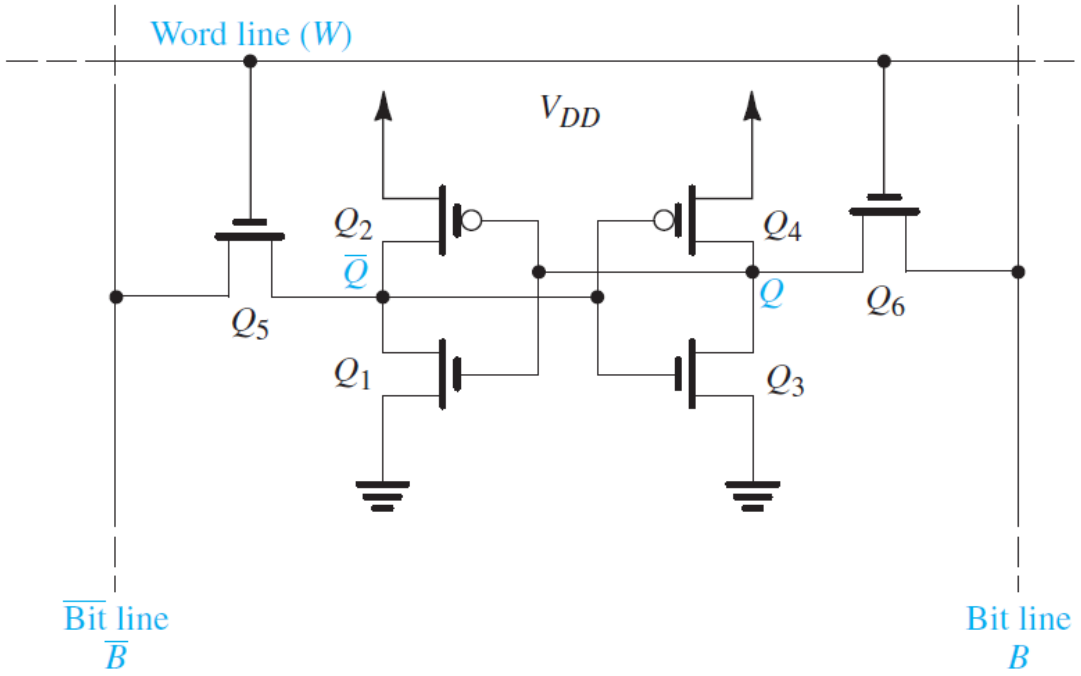
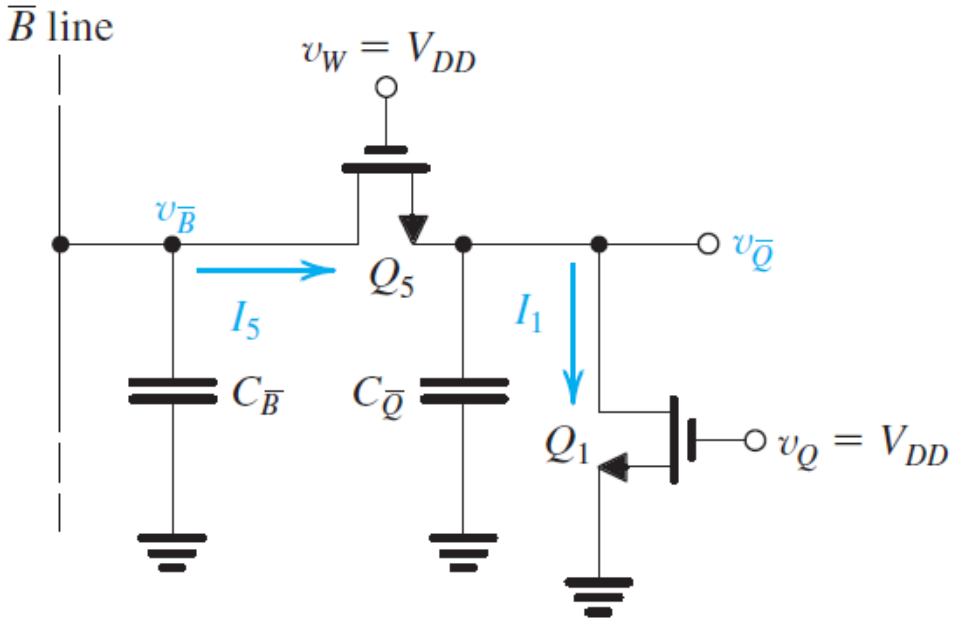


Figure 16.12 A CMOS SRAM memory cell.

The Read Operation

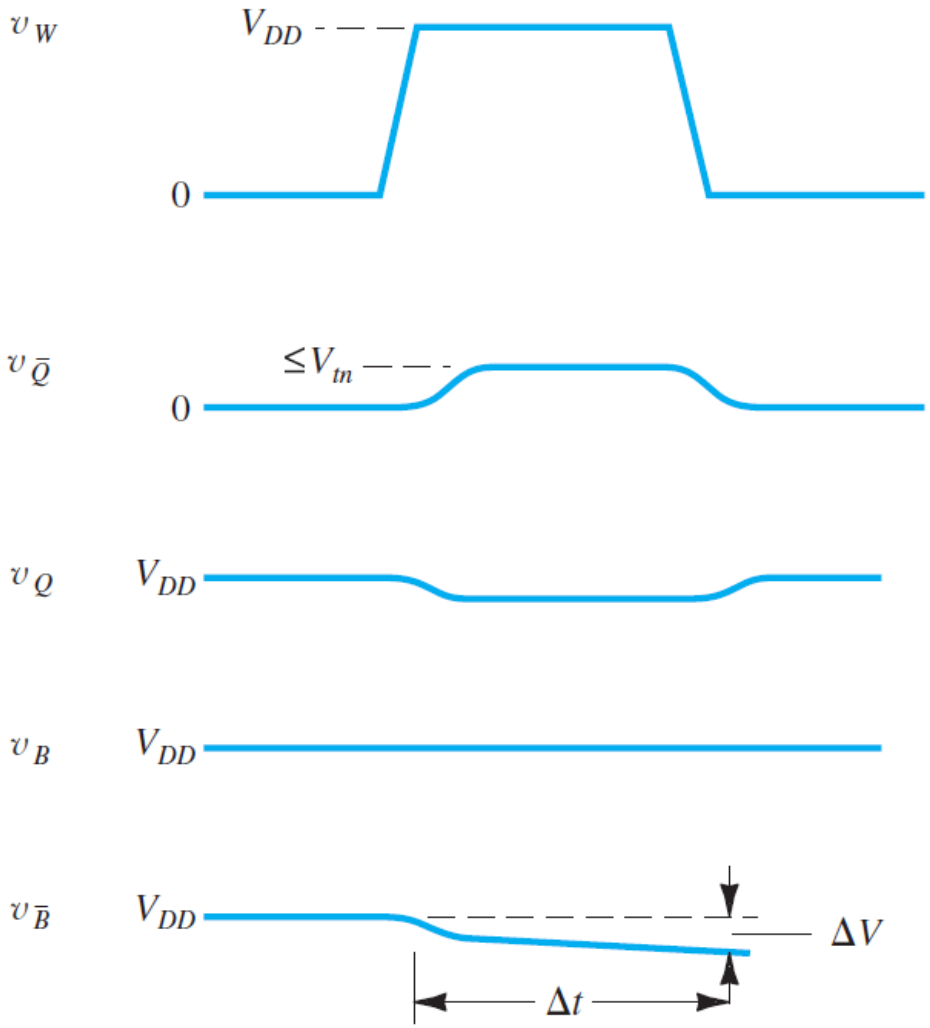
Assume that the cell is storing a "1",
$Q = V_{DD}$, $\bar{Q} = 0$

Precharge: raise the bitline, $B = \bar{B} = V_{DD}$
Turn on Q_5 and Q_6
Current I_5 flow through Q_5 into $C_{\bar{Q}}$
$v_{\bar{Q}}$ rises, Q_1 conducts,
Reach equilibrium when $v_{\bar{Q}} = V_{\bar{Q}}, I_5 = I_1$
the sense amplifier detects a minimum decrement ΔV as the presence of "1".



Static Memory (SRAM) Cell

a flip-flop



The Read Operation

Assume that the cell is storing a "1",
$Q = V_{DD}$, $\bar{Q} = 0$

Precharge: raise the bitline, $B = \bar{B} = V_{DD}$
Turn on Q_5 and Q_6
Current I_5 flow through Q_5 into $C_{\bar{Q}}$
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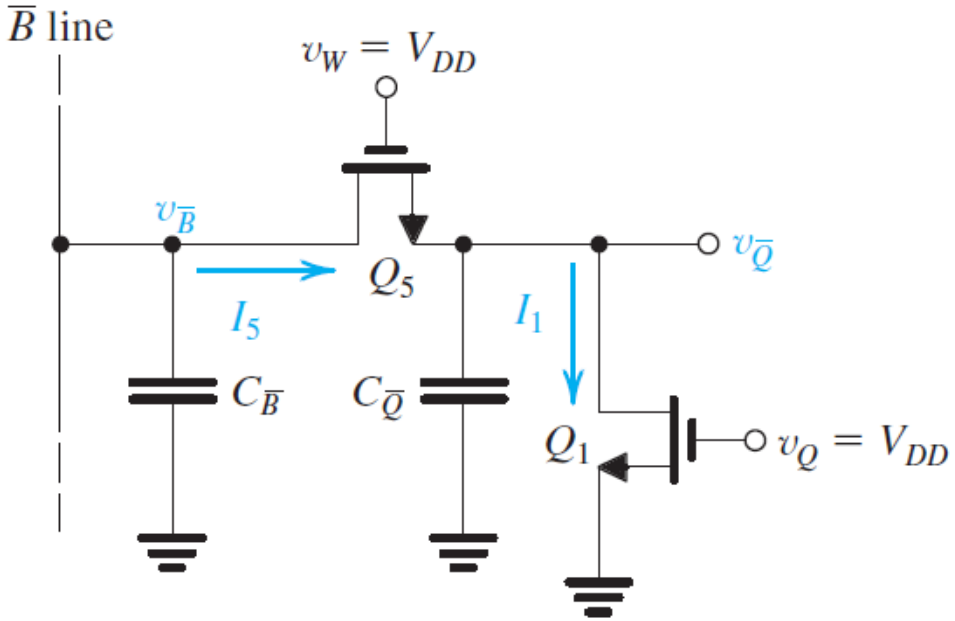
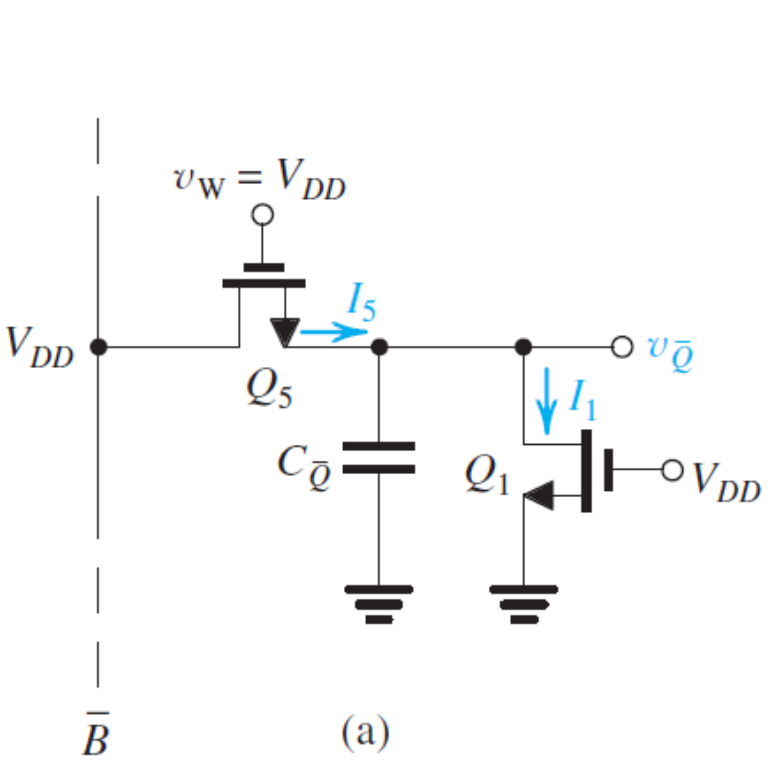
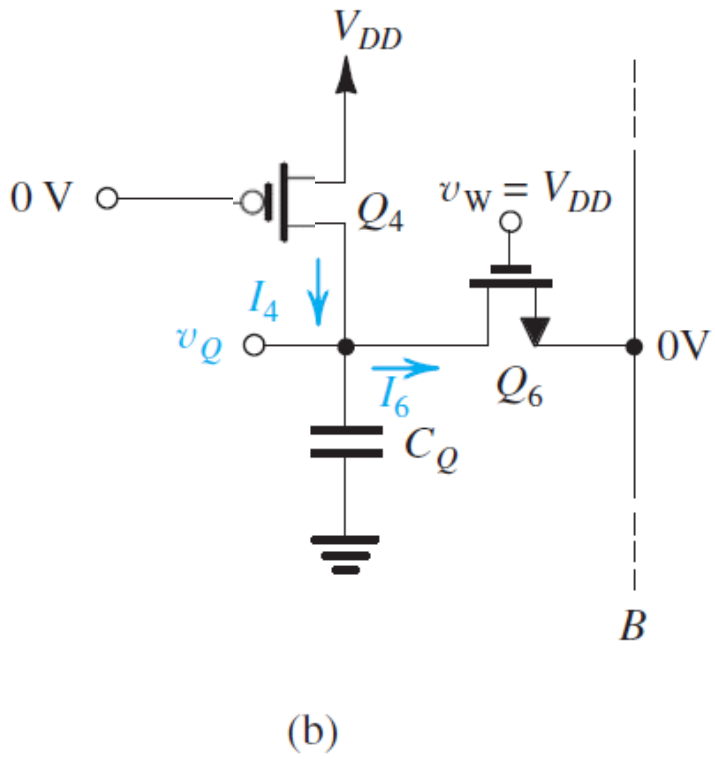


Static Memory (SRAM) Cell

a flip-flop





The Write Operation

Assume that the cell is storing a "1",
$v_Q = V_{DD}$, $v_{\bar{Q}} = 0$

To write a "0"

$$B = 0, \bar{B} = V_{DD}$$

Select a cell,

$$v_W = V_{DD}$$

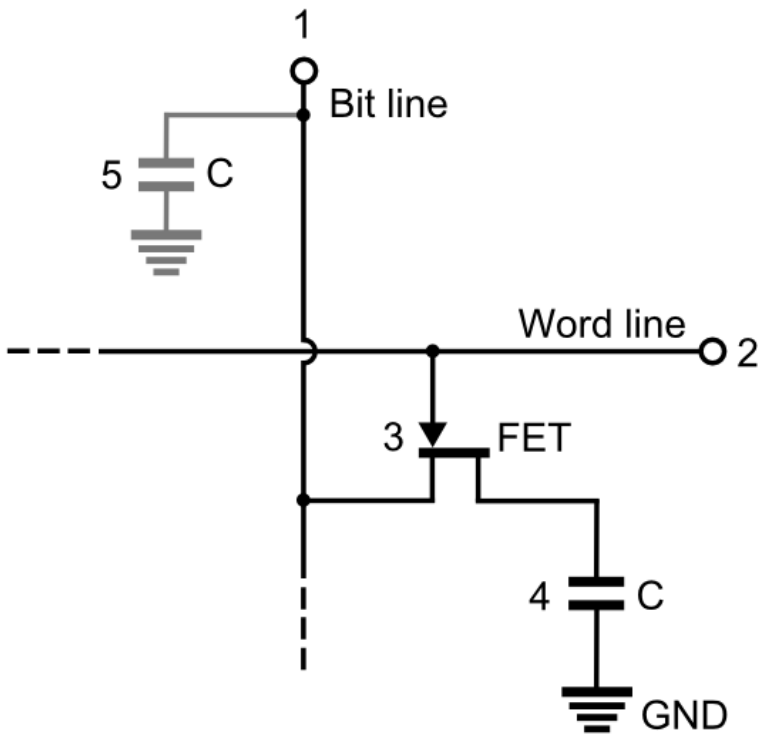
As Q_6 turns on, C_Q discharge,
v_Q begins to fall,
Q_4 conducts,
Equilibrium is reached when $I_4 = I_6$.

$$v_Q < V_{tn}$$

Due to regeneration, the cell is toggled to "0" state.

Dynamic Memory (DRAM) Cell

a bit, 0 or 1, low or high voltage



one-transistor cell

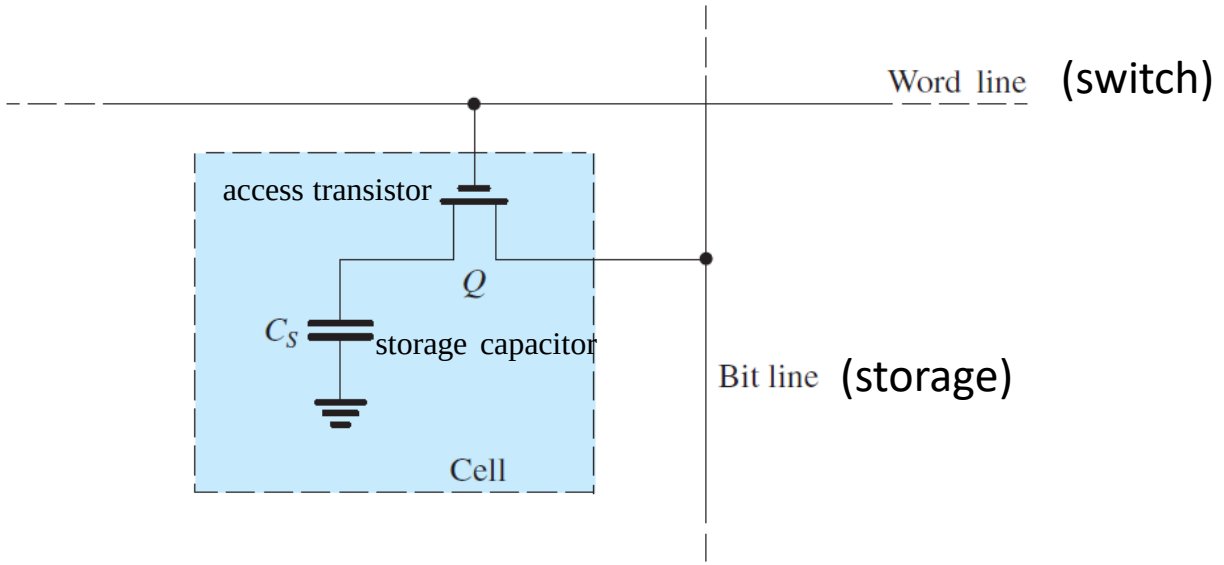


Figure 16.18 The one-transistor dynamic RAM (DRAM) cell.

When the cell is storing a 1, the capacitor is charged to V_{DD}; when a 0 is stored, the capacitor is discharged to zero volts

How the capacitor can be charged to the full supply voltage V_{DD}?

a write-1 operation:
Word line = $V_{DD} + V_t$
Bit line = V_{DD}
Start charging C_s
C_s will reach V_{DD}

Refresh:
The cell content is read,
the data bit is rewritten,
restoring the capacitor voltage to its proper value
refresh operation must be performed every 5 ms to 10 ms.

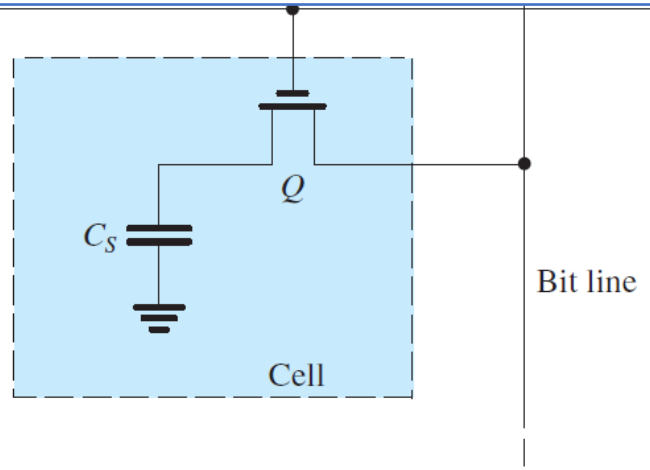


Figure 16.18 The one-transistor dynamic RAM (DRAM) cell.

Read operation:
the bit line is precharged to $V_{DD}/2$.
Assume a "1" is stored,

$$V_{CS} = V_{DD}$$

Due to charge conversation,

$$C_S V_{CS} + C_B \frac{V_{DD}}{2} = (C_B + C_S)\left(\frac{V_{DD}}{2} + \Delta V\right)$$

where ΔV is the change in the voltage on the bit line

$$\Delta V(1) \simeq \frac{C_S}{C_B}\left(\frac{V_{DD}}{2}\right)$$

If $V_{DD} = 1.8$ V, $\Delta V(1)$ will be +90 mV,
$\Delta V(0)$ will be about –90 mV

Read is destructive,

Read operation

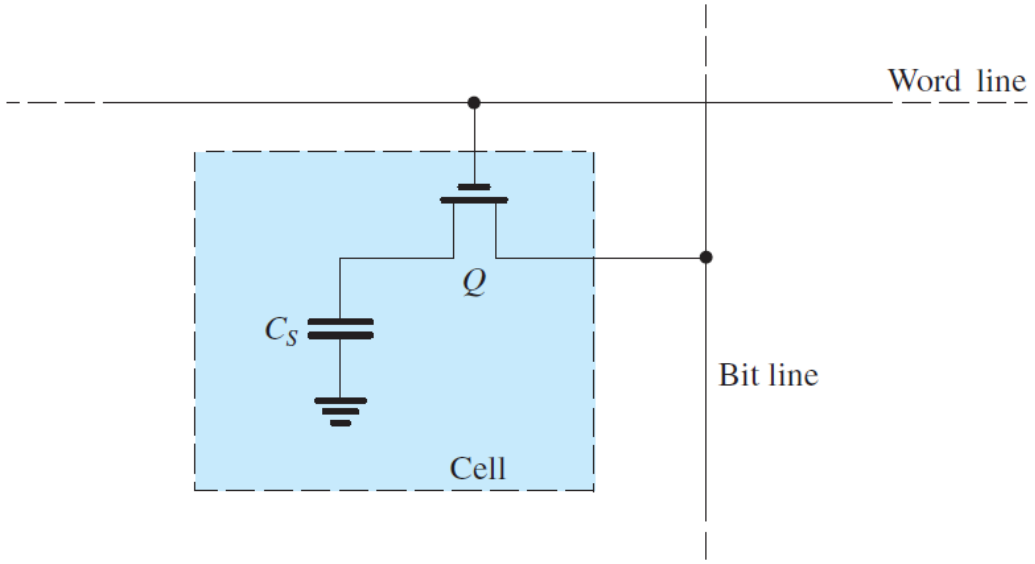


Figure 16.18 The one-transistor dynamic RAM (DRAM) cell.

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$$C_S V_{CS} + C_B \frac{V_{DD}}{2} = (C_B + C_S)\left(\frac{V_{DD}}{2} + \Delta V\right)$$

where ΔV is the change in the voltage on the bit line

$$\Delta V(1) \simeq \frac{C_S}{C_B}\left(\frac{V_{DD}}{2}\right)$$

Read is destructive,

C_s will be no longer V_{DD},

ΔV is amplified by the column sense amplifier

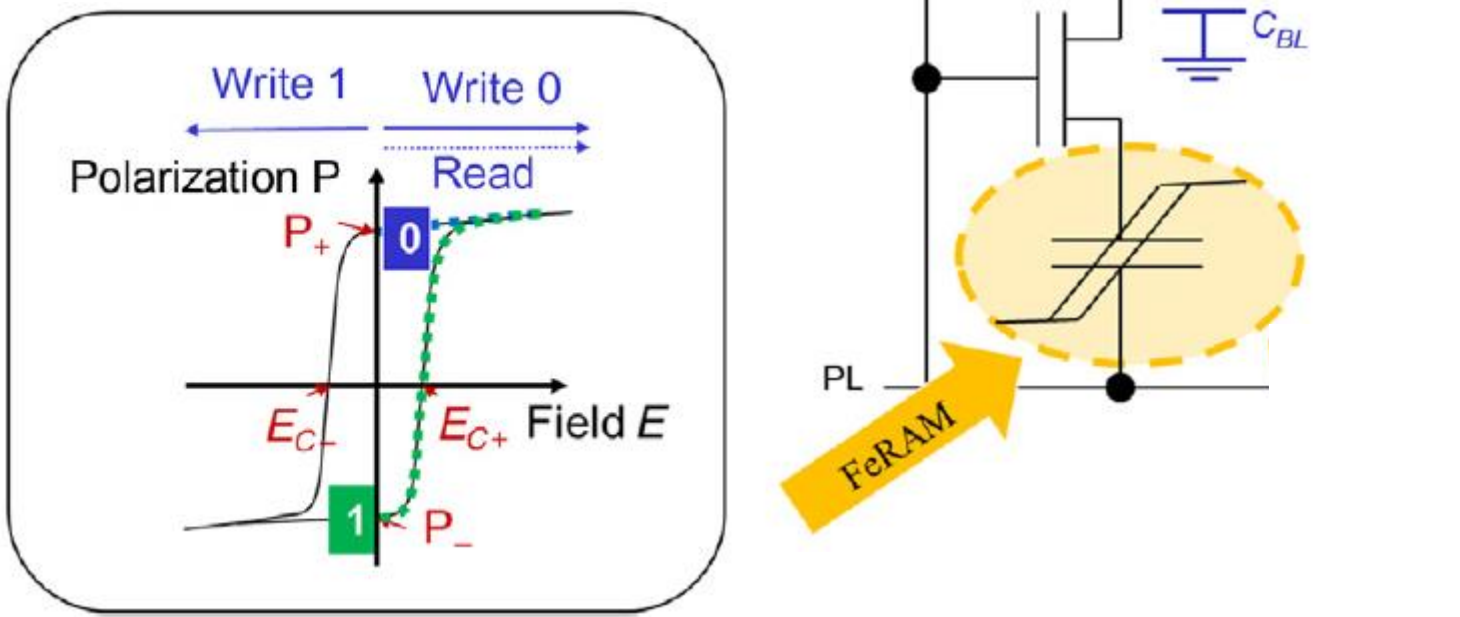
This amplified signal will restore C_s to V_{DD}

All the cells in the selected row are refreshed.

Ferroelectric RAM

non-volatile random-access memory

a memory cell is the one transistor - one capacitor (1T-1C) approach that is comparable with a DRAM where the capacitor dielectric is replaced by the ferroelectric



How does a ferroelectric random-access memory (FeRAM) work?

Thank you!

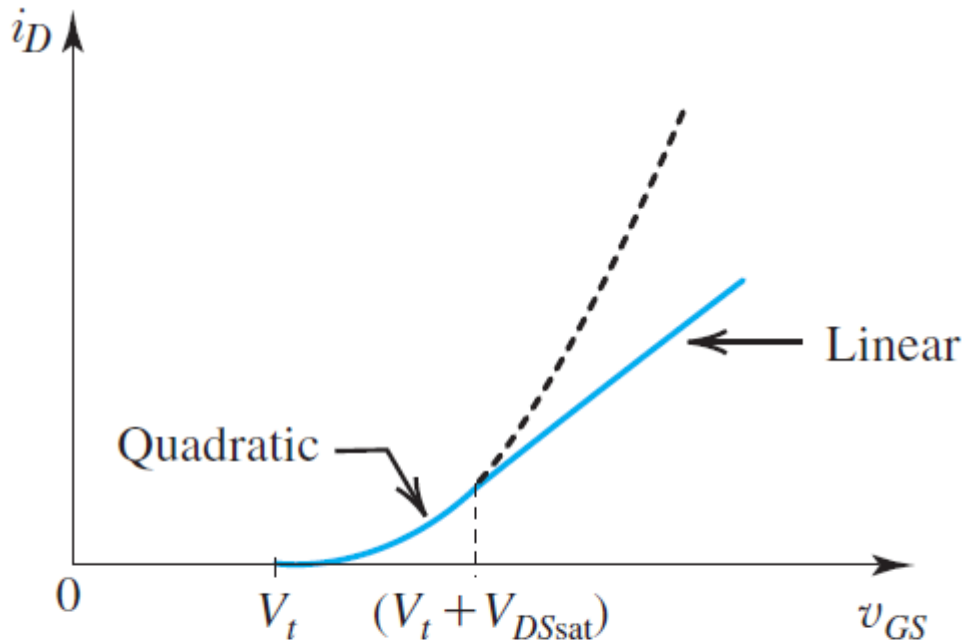


Figure 15.5 The i_D–v_{GS} characteristic of a short-channel NMOS transistor operating at $v_{DS} > V_{DSsat}$. Observe the quadratic and the linear portions of the characteristic. Also note that in the absence of velocity saturation, the quadratic curve would continue as shown with the broken line.

Dynamic random-access memory (DRAM)

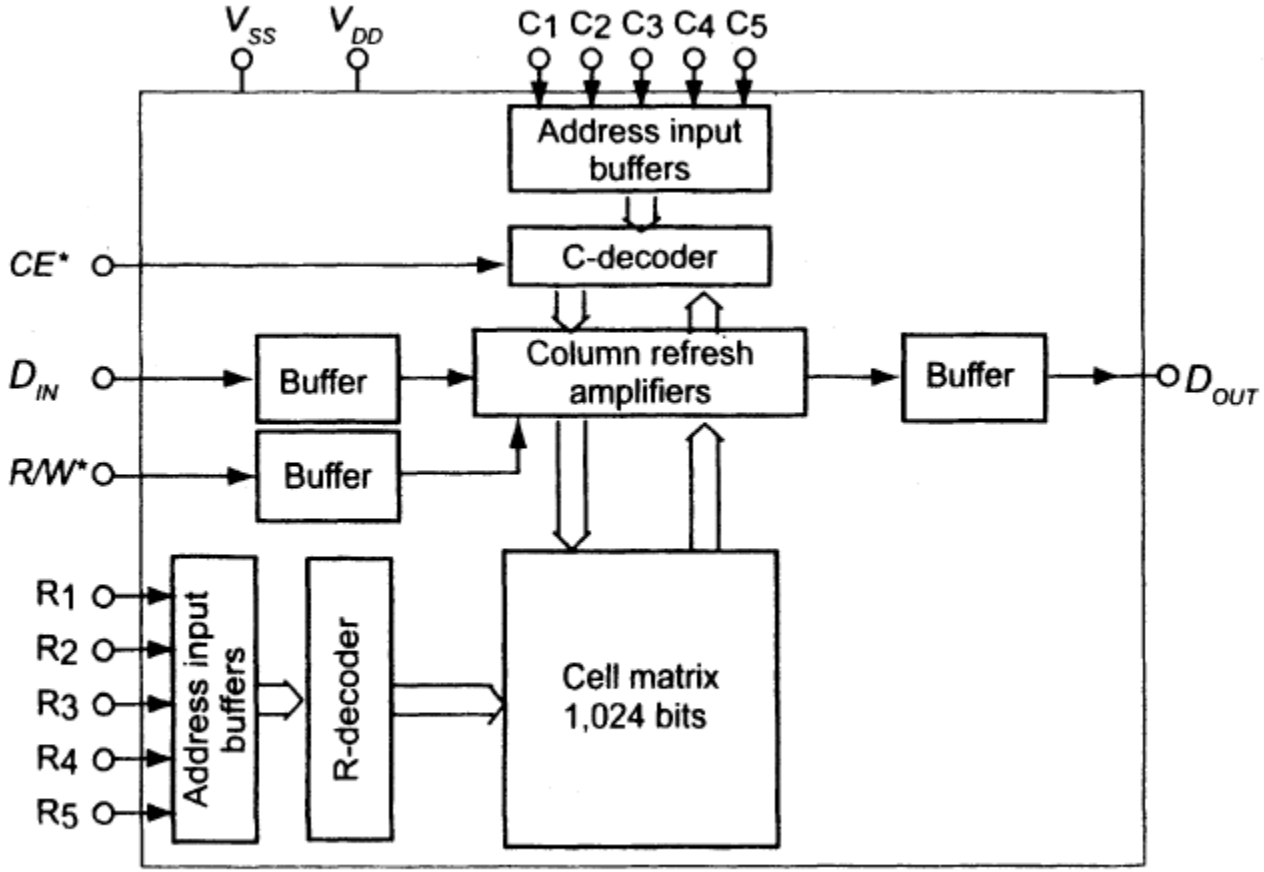
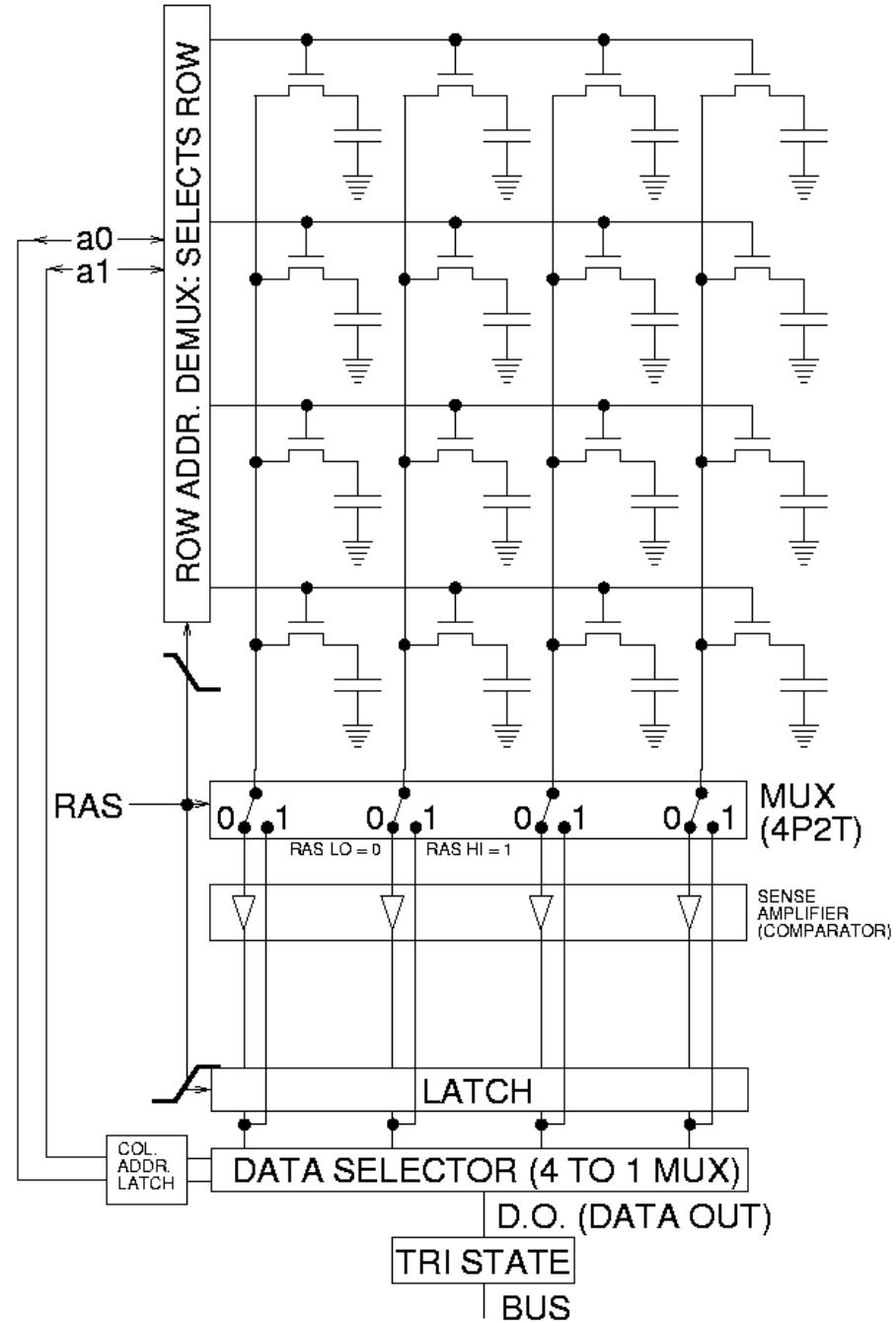


Figure 1.1 1,024-bit DRAM functional diagram.



a simple example with a four-by-four cell matrix

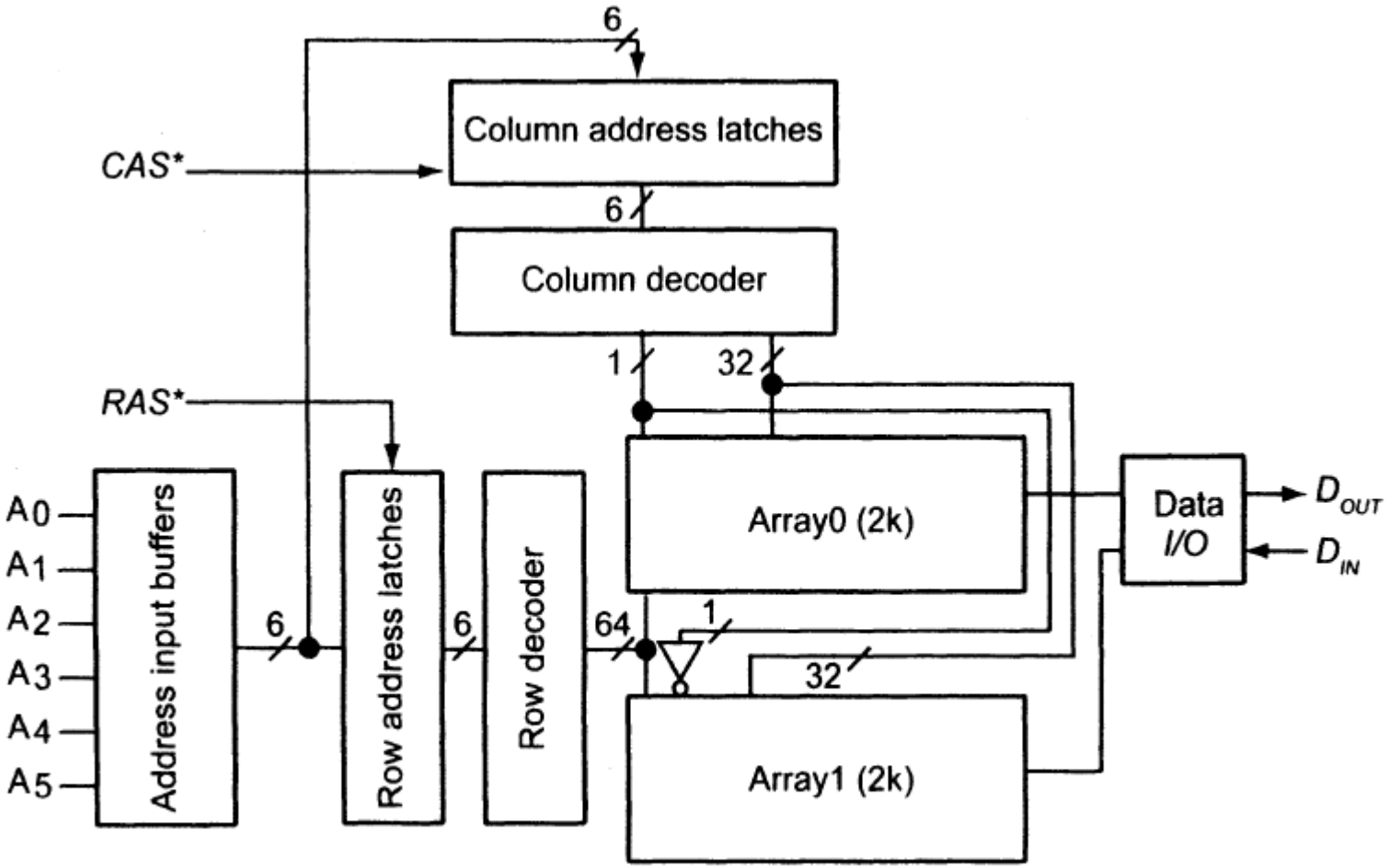


Figure 1.9 Block diagram of a 4k DRAM.

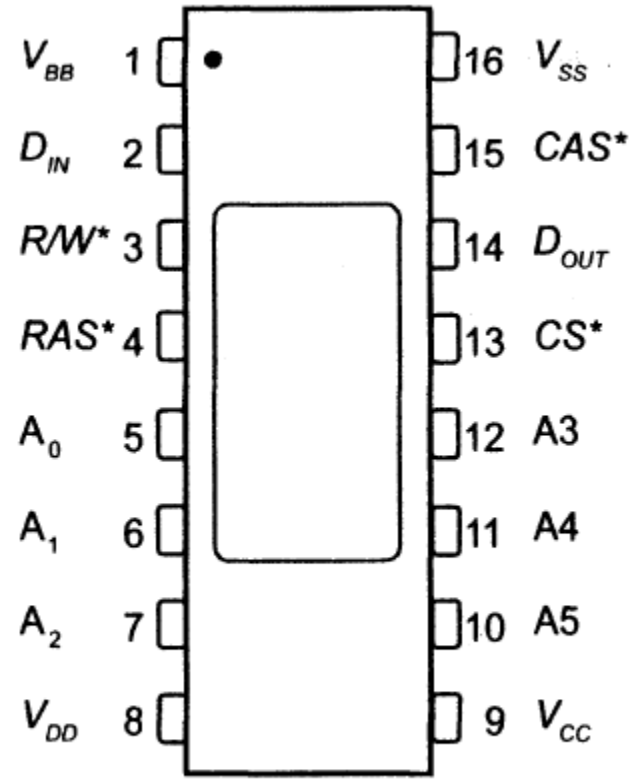


Figure 1.10 4,096-bit DRAM pin connections.